Building a Multi Core Processor and Understanding Why it Works

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Abstract: in a series of 10 lectures we present the gate level construction of a multicore processor with MIPS instruction set and pipelined processor cores. We explain why it works simply by mathematical correctness proof.

Prerequisites: students should be comfortable with high school mathematics and with proofs by induction. Some familiarity with Boolean Algebra will be helpful; previous classes in hardware design and computer architecture are not required.

Course Outline

day 1: numbers, Boolean formulae, circuits, hardware models, control automata, multi port RAMs

day 2: ALU design, MIPS instruction set, sequential processor design

day 3: Pipelining, forwarding, hardware interlock

day 4: Caches, MOESI cache coherence protocol, shared memory implementation

day 5: Correctness of the shared memory implementation; integration of processor pipelines.

Interested students can find an almost complete preview of the lecture notes at

http://www-wjp.cs.uni-saarland.de/lehre/vorlesung/rechnerarchitektur2/ws1112/layouts/multicorebook.pdf

The gaps in the lecture notes can be filled in by reading chapter 4 of:

S. Müller, W. J. Paul, Computer Architecture. Springer Verlag, 2000